AMENDMENTS TO THE CLAIMS

Applicant submits below a complete listing of the current claims, including marked-up claims with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing. This listing of claims replaces all prior versions, and listings, of claims in the application:

Listing of the Claims

1. (Currently amended) [[0]]A monitoring device integrated on [[the]] a chip of a microprocessor executing a sequence of instructions, comprising:

a message calculation means for, on each execution of an instruction from among a plurality of instructions of predetermined types, generating a digital message corresponding to a type of the executed instruction;

a buffer memory for storing each generated message; and

a plurality of output terminals connected to an external analysis tool, each output terminal being associated with one of the instruction types and the message calculation means modifying [[the]] a state of the output terminal associated with an instruction type ~~at the time~~ when a message corresponding to said instruction type is stored in the buffer memory so that the external analysis tool stores a time when the state of the output terminal is modified.

2. (Currently amended) The monitoring device of claim 1, wherein the buffer memory is divided into ~~several~~ a plurality of areas, each of ~~which~~ the areas is associated with a different instruction type and is intended to only store messages associated with said instruction type.

3. (Previously presented) The monitoring device of claim 1, wherein each output terminal is connected to a test terminal.

4. (Currently amended) The monitoring device of claim 1, wherein each output terminal is connected to an input terminal of a coding block comprising a predetermined number

of coding block output terminals, each of ~~which~~ the coding block output terminals is connected to a test terminal[[;]], each coding block being provided to have each of its n coding block output terminals switch once every n state switchings of its input terminal and so that a single one of its n coding block output terminals switches state at once.

5. (Currently amended) The monitoring device of claim 1, wherein only certain types of instructions ~~only~~ are associated with an output terminal of the message calculation means.

6. (Currently amended) The monitoring device of claim 1, wherein each of the possible instruction types is associated with an output terminal of the message calculation means.

7. (Currently amended) An integrated circuit comprising:

a microprocessor for executing a sequence instructions; and

a monitoring device ~~of claim 1~~ for monitoring the execution of the sequence of instructions, the monitoring device comprising:

a message calculation means for generating digital messages, wherein each digital message corresponds to a predetermined type of an instruction from a plurality of predetermined instruction types, and wherein the digital message is generated on each execution of the instruction of the predetermined type,

a buffer memory for storing the generated digital messages; and

a plurality of output terminals connected to an external analysis tool, wherein an output terminal from the plurality of output terminals is associated with an instruction type and the message calculation means modifying a state of the output terminal when a digital message corresponding to the instruction type is stored in the buffer memory so that the external analysis tool stores a time when the state of the output terminal was modified.

8. (Currently amended) A method for monitoring a microprocessor executing a sequence of instructions by means of a device integrated to [[the]] a microprocessor chip, the method comprising:

on each execution of an instruction from the sequence of instructions, generating a digital message corresponding to a type of the executed instruction; and

storing each generated digital message in a buffer memory; and

modifying [[the]] a state of one of a plurality of output terminals connected to an external analysis tool and each associated with an instruction type when a digital message corresponding to the instruction type to which said output terminal is associated is stored in the buffer memory.

9. (New) The method of claim 8, wherein the buffer memory is divided into a plurality of areas, with each area from the plurality of areas storing digital messages associated with an instruction type.

10. (New) The integrated circuit of claim 7, wherein the buffer memory is divided into a plurality of areas, with each area from the plurality of areas storing digital messages associated with an instruction type.

11. (New) The integrated circuit of claim 7, wherein each output terminal is connected to a test terminal.

12. (New) The integrated circuit of claim 11, wherein a state of the test terminal is modified when a state of the output terminal connected to the test terminal is modified.

13. (New) The integrated circuit of claim 7, wherein, when at least two instructions of a first and a second type from the sequence instructions are executed in parallel, the message calculation means generates a digital message corresponding to an instruction of a first type and modifies a state of an output terminal associated with the instruction of the first type and simultaneously generates a digital message corresponding to an instruction of a second type and modifies a state of an output terminal associated with the instruction of the second type.

14. (New) The integrated circuit of claim 13, wherein the external analysis tool stores a time when the state of the output terminal associated with the instruction of the first type was modified and a time when the state of the output terminal associated with the instruction of the second type was modified.

15. (New) The integrated circuit of claim 7, wherein each output terminal is connected to an input terminal of a coding block comprising a predetermined number of coding block output terminals, each of the coding block output terminals is connected to a test terminal, wherein a state of a coding block output terminal switches once per the predetermined number of times a state of the input terminal switches, and wherein the predetermined number of the coding block output terminals switch states one at a time.

16. (New) The integrated circuit of claim 7, wherein each output terminal from the plurality of output terminals is associated with a plurality of instruction types.

17. (New) The integrated circuit of claim 7, wherein each instruction type is associated with an output terminal.